MONOLITHIC AND DISCRETE MM-WAVE InP LATERAL TRANSFERRED-ELECTRON OSCILLATORS

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ABSTRACT

We have investigated a lateral InP transferred-electron device structure and demonstrated its application to mm-wave monolithic integrated circuits (MMICs). From cavity-tuned discrete devices, the highest CW power output (29.1 mW) and conversion efficiency (6.7%) of any lateral transferred-electron device has been obtained at 29.9 GHz. These devices also had a CW power output of 0.4 mW at 98.5 GHz and a CW power output of 0.9 mW at 75.2 GHz. In addition, the first monolithic oscillator incorporating a lateral transferred-electron device has been demonstrated at 79.9 GHz.

INTRODUCTION

The material properties of InP are excellent for transferred-electron device operation in the mm-wave region (1). As a result, mm-wave InP high efficiency oscillators and low-noise broadband amplifiers have been demonstrated (2,3). The device structures typically used have the current flow perpendicular to the wafer surface and employ n^+ substrates or thick n^+ layers grown on semi-insulating substrates. The presence of n^+ substrates or thick n^+ layers makes monolithic integration with other devices difficult to achieve. This work focuses on the development of a lateral transferred-electron device structure which is more suitable for integration in mm-wave monolithic circuits.

We have previously reported on X-band (8.2 - 12.4 GHz) lateral InP transferred-electron oscillators which had a localized high resistivity region self-aligned to the cathode contact (4,5). The high resistivity region, referred to as a notch, partially extended into the active layer and was formed by selective implantation damage. This device design was implemented to create a localized high electric field region, which would produce a laterally-uniform, well-defined space charge nucleation site. The notched devices demonstrated significantly superior microwave performance as compared to devices without a notch. At X-band the notched devices operated with dc-to-RF conversion efficiencies of up to 9.5 percent while the devices without a notch operated with efficiencies of less than 1 percent.

In this letter, we report on recent advances in lateral transferred-electron device technology and its application in mm-wave monolithic circuits. From cavity-tuned discrete devices a CW power output of 29.1 mW with a dc-to-RF conversion efficiency of 6.7% has been demonstrated at 29.9 GHz. At W-band, CW power outputs of 0.9 mW and 0.4 mW have been obtained at 75.2 GHz and 98.5 GHz, respectively. An 80 GHz monolithic oscillator incorporating the lateral transferred-electron device will also be described.

Discrete Device Design and Fabrication

The device cross section is shown in Fig. 1 and the discrete device lay-out is shown in Fig. 2. The devices were fabricated with a notch length of 0.4 μm and cathode-to-anode spacings of 1.5 and 2.7 μm. The width of the discrete devices was 100 μm and the width of the devices used in the monolithic oscillator was 200 μm. The width of 200 μm was chosen for optimum negative resistance magnitude and as a reasonable compromise between device thickness and resonator width. The material used was n-type vapor phase epitaxial InP grown with an unintentionally doped buffer layer on an Fe-doped semi-insulating substrate. For the discrete devices the active layer carrier concentration was 3×10^{16} cm^{-3} with a thickness of 0.9 μm. For the monolithic oscillator the active layer carrier concentration was 5×10^{16} cm^{-3}. These carrier concentrations and thicknesses were chosen to exceed the nl and nd products of 10^{13} cm^{-2} and 10^{12} cm^{-2}, respectively (6). To begin device fabrication (7), the cathode and anode metallization patterns were defined in photoresist and AuGe/Au (1000 Å/1000 Å) was slant evaporated at an angle of approximately 25°. Using the metallization as a mask, oxygen was implanted at an energy of 50 keV and a fluence of 3.0×10^{11} cm^{-2} into the regions that were left exposed after the slant evaporation. The resistivity of oxygen-implanted InP has been measured to be 10^3 ohm-cm and is thermally stable to 450°C (8). Using the implantation parameters for oxygen into InP (9) and the resistivity of the oxygen-implanted InP as a function of fluence (8), the notch depth is determined to be 0.25 μm. After the oxygen implantation the cathode and anode patterns were defined by lift-off. The sample was then alloyed on a hot plate at 420°C for 60 seconds in a N_2/H_2 90/10% ambient. Device mesas were etched in a

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(1000:80:6:1 H_2O:HBr:KBr:Br_2) solution. The device bonding pads shown in Fig. 2 were formed by the lift-off of Cr/Au (50/4000 Å). The wafers were then lapped to 100 μm and the individual devices were scribed and separated.

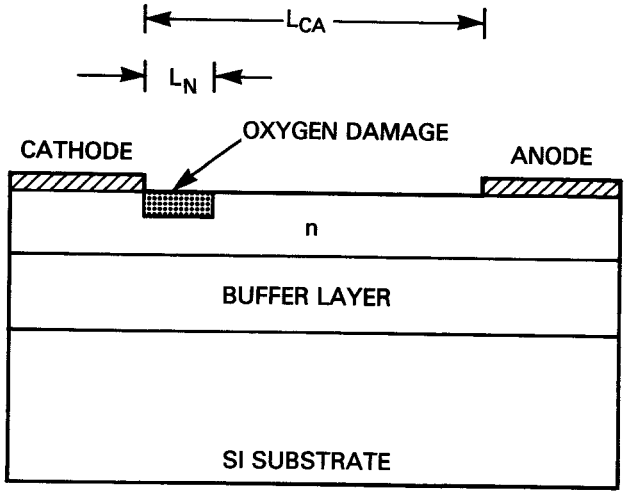

Figure 1. Discrete device cross section. The notch length, L_N, was 0.4 μm and the cathode to-anode spacing, L_{CA}, was 1.5 μm and 2.7 μm.

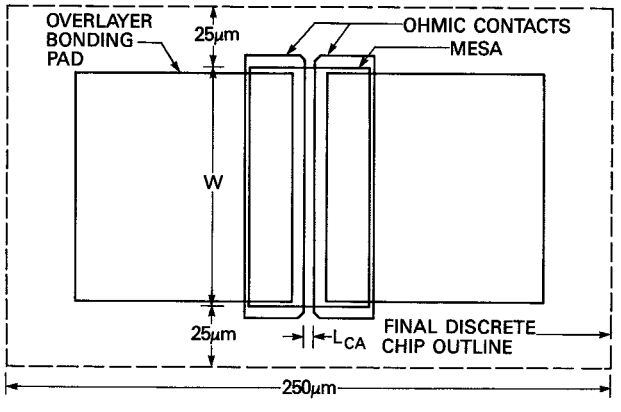

Figure 2. Discrete device lay-out.

Monolithic Oscillator Design and Fabrication

The cross section of the device used in the monolithic oscillator is shown in Fig. 3 and the top view of the monolithic oscillator lay-out is shown in Fig. 4. In addition to the differences of device width and carrier concentration described above, the devices used in the monolithic oscillator were fabricated with an n^+ anode. The n^+ anode was formed by the selective ion implantation of Si at energies of 30, 100, and 250 keV with fluences of 0.86, 2.2, and 6.6 x 10^{13} cm^{-2}, respectively. To activate the n^+ implant the sample was proximity annealed at 725°C for 15 min in a N_2/H_2 90/10% ambient. This procedure produces a layer with a carrier concentration of 1 x 10^{18} cm^{-3} and a room temperature Hall mobility of 1900 cm^2/V-sec. The distance from the cathode contact to the n^+ implanted region is 2.0 μm. The distance from the edge of the n^+ implanted region to the anode metallization is 1.5 μm. The other difference in the fabrication of the monolithic oscillators was that the circuit metallization pattern shown in Fig. 4 was used in place of the discrete device bonding pads. The circuit metallization was formed by the lift-off of Cr/Au (50/6000 Å). After the circuit metallization was lifted, the wafer was lapped to a thickness of 75 μm. One micron of Al was evaporated to form the microstrip ground plane. The final chip size of the monolithic oscillators was 1.5 mm by 1.6 mm.

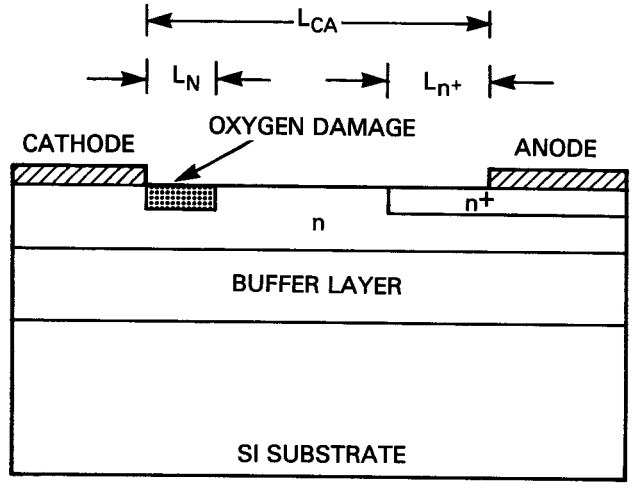

Figure 3. Cross section of device structure used for the monolithic oscillator. The notch length, L_N, was 0.4 μm. The cathode-to-anode spacing was 3.5 μm, and the n^+-to-anode spacing, L_N^+, was 1.5 μm.

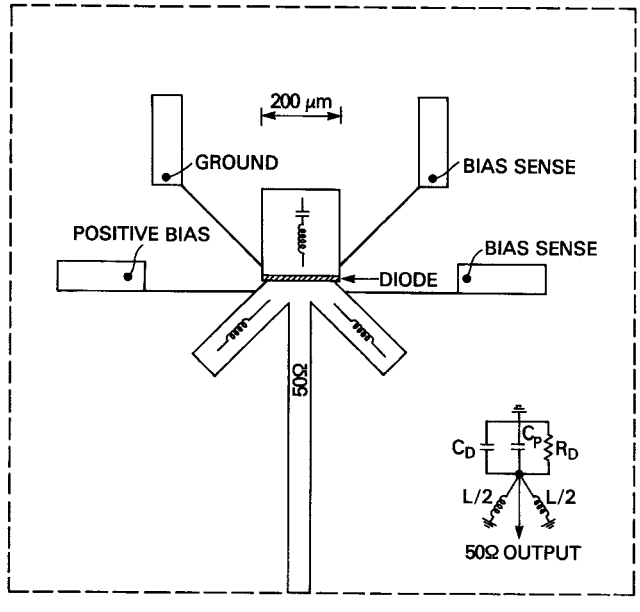

Figure 4. Monolithic oscillator lay-out with an equivalent circuit shown in the inset.

The monolithic oscillator was designed by assuming a diode equivalent circuit of an active negative resistance, Rd, in parallel with an active capacitance, Cd, as shown in the inset of Fig. 4. The parasitic capacitance, Cp, shown in that figure is predominantly the capacitance between the surface metallization on opposite sides of the diode. The parasitic capacitance was calculated to be 0.12 pF. The diode area was chosen to make Rd approximately -50 ohms, and the active diode capacitance used was approximatly 0.1 pF according to (10).

The distributed circuit of Fig. 4 was formulated so that the magnitude of the device negative resistance would equal the load resistance and that the reactance of the diode and parasitic capacitance would equal the reactance of the shunt inductance. The designs were for a substrate thickness of 75 μm and a dielectric constant of 12.55 was used for the semi-insulating InP. The RF short circuit on one side of the InP device was provided by a quarter wavelength open circuited stub whose characteristic impedance was 24 ohms and whose dissipation loss was 0.27 dB per wavelength. The length of this line, and of all the other open circuited lines, was corrected for end-fringing capacitance. The shunt inductance at the other side of the InP device was provided by the two identical open circuited stubs, having a characteristic impedance of 43 ohms and loss of 0.31 dB per wavelength. The total equivalent inductance was selected to resonate at the desired operating frequency with the 0.22 pF of total capacitance estimated for the sum of the active diode capacitance and the parasitic capacitance. The distributed circuit is made physically symmetrical to help assure that the RF field pattern in the diode and in the RF grounding stub remains in the dominant quasi-TEM configuration (not in a laterally asymmetrical mode). The transmission line circuitry was computer optimized with losses included in the analysis.

The dc bias circuitry uses quarter wavelength transmission lines of high (120 ohm) and low (42 ohm) characteristic impedance. The physical symmetry is maintained by using bias connections on both sides of the circuit. In operation, one set of bias leads has the bias supply attached and the other set is used for sensing. This arrangement is useful because at high current levels the voltage drop in the high impedance bias lines is not negligible and the correct diode voltage must be measured at the bias sensing terminals.

Discrete Device Evaluation

For discrete device evaluation, devices were wirebonded into diode packages. The packaged diodes were then inserted into a tunable waveguide cavity. The dc I-V characteristics of a 2.7 μm and 1.5 μm device while operating in a tuned circuit are shown in Fig. 5. CW operation is possible for the values of carrier concentration and thickness chosen. The lower threshold current level for the shorter device is attributed to a variation in carrier concentration across the wafer. Above an applied voltage of 7 and 12 volts for the 1.5 μm and 2.7 μm device lengths, respectively, the devices burn out. The current level in the negative differential resistance region depends on circuit tuning.

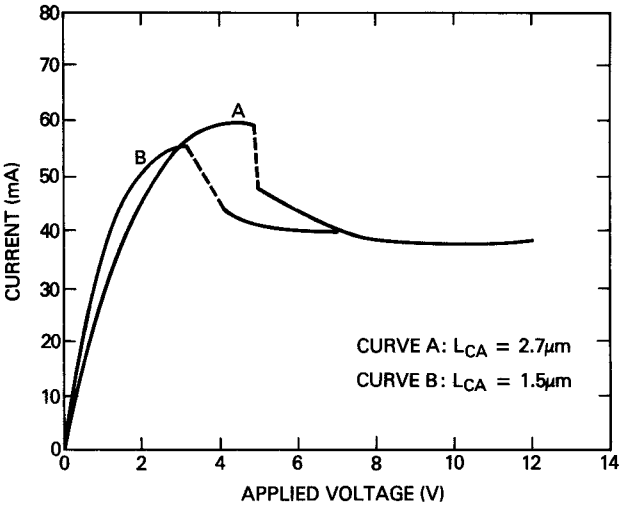

Figure 5. dc I-V characteristics of 1.5 μm and 2.7 μm long devices while operating in a tuned waveguide cavity.

The device with a 2.7 μm length was tested in a Ka-band (26.5-40.0 GHz) tunable waveguide cavity. This device demonstrated a CW power output of 29.1 mW with a dc-to-RF conversion efficiency of 6.7% at a frequency of 29.9 GHz. This high level of efficiency in this frequency range is a factor of ten higher than that of InP control devices fabricated without a notch and other GaAs lateral transferred-electron device structures (11). This result represents a significant advance toward achieving the efficiency of 13% currently obtained with current-limiting InP mesa-structure transferred-electron devices (12). Devices with a cathode-to-anode spacing of 1.5 μm have been tested at W-band (75-110 GHz). A CW power output of 0.4 mW with an efficiency of 0.2% at 98.5 GHz and a CW power output of 0.9 mW with an efficiency of 0.4% at 75.2 GHz has been achieved. This is believed to be the highest reported oscillation frequency obtained from a lateral transferred-electron device.

Monolithic Oscillator Evaluation

To evaluate the monolithic oscillator, the 1.5 mm by 1.6 mm chip was mounted onto a brass test fixture. The 50 ohm microstrip output line was connected to the inner conductor of a coaxial line which then transitioned to W-band waveguide (13). Due to high current levels, the device was tested with 1 μsec pulses at 1% duty cycle to prevent thermal burn-out. The threshold current level was 350 mA and the operating current was 245 mA. The threshold voltage was 7 volts and the operating voltage was 13 volts. There was a

resistance of eight ohms in the bias line connections. Without external tuning, the circuit oscillated at 79.9 GHz with a pulsed power output of 0.1 mW. The design frequency for this oscillator was 75 GHz. A waveguide tuner was used, but no more power could be achieved with external tuning. Therefore, the circuit has produced approximately the correct frequency and approximately the correct load resistance for the diode. It is expected that increased power output will be obtained with subsequent samples.

SUMMARY

In summary, we demonstrated the highest CW power output and efficiency of a lateral transferred-electron device at 30 GHz, the highest oscillation frequency of a lateral transferred-electron device, and the first monolithic oscillator incorporating a lateral transferred-electron device. These results provide incentive for further work on lateral transferred-electron devices for monolithic oscillators at 30 GHz and above.

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REFERENCES

(1) L . Wandinger, "Mm-wave InP Gunn devices: status and trends," Microwave J., pp. 71-78, Mar. 1981.
(2) B. Fank, "Indium phosphide mm-wave devices and components," Microwave J., pp. 95-101, Apr. 1984.
(3) B. Fank, J. Crowley, and C. Hang, "InP Gunn diode sources, "Proceedings of SPIE, Vol. 544, Mm-wave Tech. III, pp. 22-28, April 1985.
(4) S. C. Binari, H. L. Grubin, and P. E. Thompson, "Notched InP planar transferred-electron oscillators," in IEDM Tech. Dig., 1982. pp. 770-773.
(5) S. C. Binari, P. E. Thompson, and H. L. Grubin, "Self-aligned notched planar InP transferred-electron oscillators, "IEEE Electron Device Lett., Vol. EDL-6, No. 1, Jan. 1985, pp. 22-24.
(6) K. Mause et al., "Circuit integration with gate-controlled Gunn devices," 1972 Symp. on GaAs, pp. 275-285.
(7) More details and figures explaining device fabrication can be found in reference 5.
(8) P. E. Thompson, S. C. Binari, H. B. Dietrich, and R. L. Henry, "Device isolation by oxygen implantation in n-type indium phosphide," Solid-State Electronics, Vol. 27, Nos. 8/9, pp. 817-818, 1984.
(9) J. F. Gibbons, W. S Johnson, and S. W. Mylroie, Projected Range Statistics, Semiconductors and Related Materials, 2nd ed., Stroudsburg, PA: Dowden, Hut chinson, and Ross, 1975.
(10) J. A. Copeland, "Theoretical study of a Gunn diode in a resonant circuit, " IEEE Trans. Electron Devices, vol. ED-14, pp. 55-58, Feb. 1967.
(11) R. Kuch et al., "Millimeter-wave operation of a 20 micron long field effect controlled transferred-electron device ("FECTED"),"1983 Inst. Phys. Conf. Ser. No. 65, pp. 439-444.
(12) J. Crowley, Varian Associates, private communication.
(13) R. E. Neidert, "Waveguide-to-coax-to micro-strip transitions for millimeter-wave monolithic circuits," Microwave J., June 1983, pp. 93-101.